

# Detector Support Group

*We choose to do these things "not because they are easy, but because they are hard".*

**Weekly Report, 2023-03-22**

## Hall A – CLEO

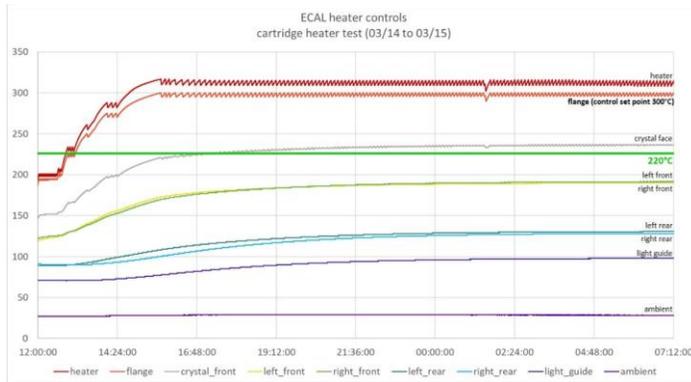
*Brian Eng*

- Updated Wi-Fi guest password on all eight field mapping units and deployed them for upcoming low power test
- Retrieved data from microSD cards of units
  - ★ Some units have bad data, with magnetic data of a single value

## Hall A – ECAL

*Brian Eng, Tyler Lemon, and Marc McMullen*

- Completed heater test, achieving 220°C at the crystal face

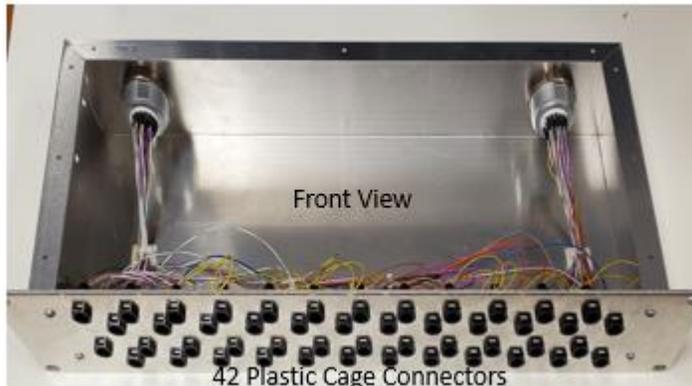


- At conclusion of test, all components were in working condition except the high temperature RTDs, which failed; standard RTDs performed as expected without visible damage
  - ★ Reviewed test results with Hall A
- Ordered controls components for the six supermodule test stand
- Using SpaceClaim, generating regions for air gaps in supermodule assembly model
- Meshing supermodule model in Fluent

## Hall A – GEp

*Mindy Leffel*

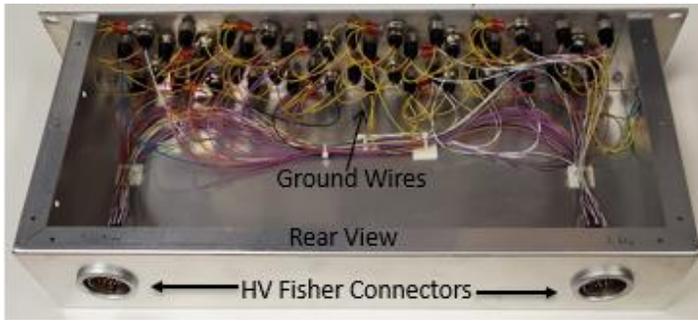
- Finished populating one high voltage patch panel; started second



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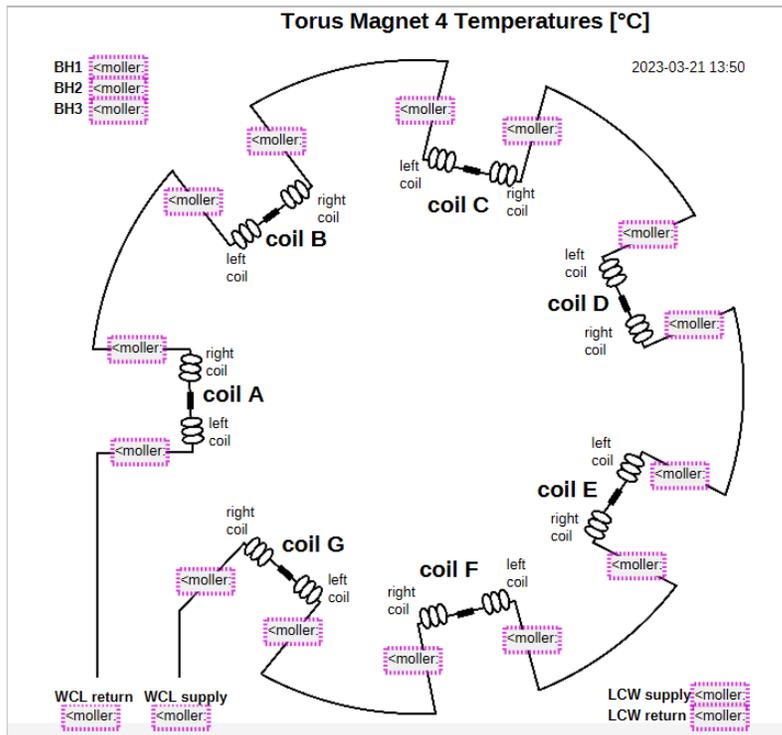
**Weekly Report, 2023-03-22**



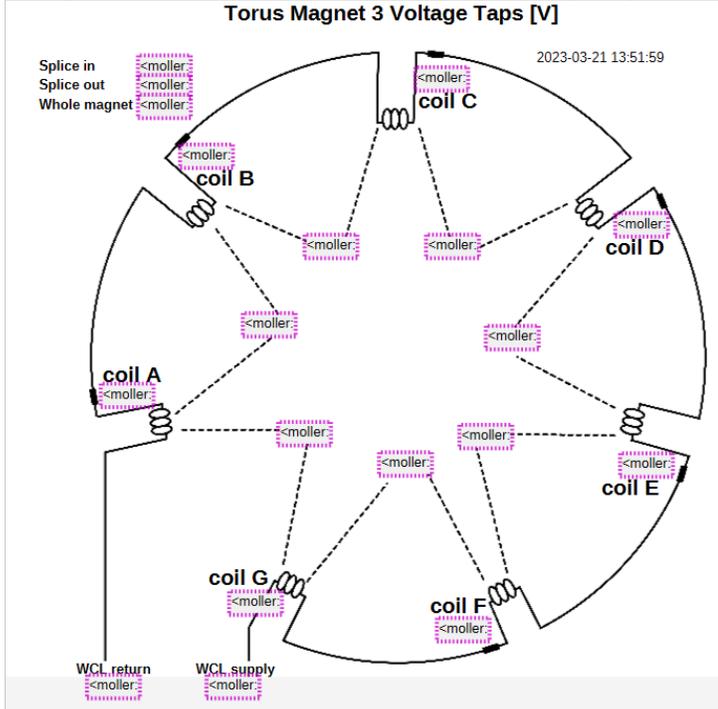
## Hall A – Møller

*Mary Ann Antonioli and Brian Eng*

- Installed EPICS on Windows machine that uses Siemens software; took three attempts to compile to include Siemens PLC driver, trying Visual Studio from Microsoft, MSYS2, and finally Windows Subsystem for Linux 2, which allowed all EPICS software to compile without errors (base + ASYN driver + s7nodave [Siemens PLC driver])
- Again, reviewed RTD drawings Kaiyi put on document control (previously rejected by others)
- Completed Phoebus screen for magnet 4 temperature display



- Completed screens for voltage display, using diagram, for magnets 1, 2, 3 (below), and 4



- Completed screens for voltage display, as a list, for magnets 1, 2, and 3

### Torus Magnet 3 Voltage Taps [V]

2023-03-21 13:53:06

Splice in	<moller:>
Splice out	<moller:>
WCL supply	<moller:>
WCL return	<moller:>
Whole magnet	<moller:>
Coil A	<moller:>
Coil B	<moller:>
Coil C	<moller:>
Coil D	<moller:>
Coil E	<moller:>
Coil F	<moller:>
Coil G	<moller:>
Coil A-B	<moller:>
Coil B-C	<moller:>
Coil C-D	<moller:>
Coil D-E	<moller:>
Coil E-F	<moller:>
Coil F-G	<moller:>
Coil G-A	<moller:>

### Hall A – SoLID

Pablo Campero

- Continued debugging warnings in FactoryTalk View data logger system of failure to reconnect automatically to the database file, due to file size



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## **Hall C – NPS**

*Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, Mindy Leffel, and Marc McMullen*

- Created new LabVIEW project for thermal readback that does not use arrays
  - ★ Determined that arrays do not have the necessary alarm levels
- Created new LabVIEW EPICS server
- Developing a Python program to save and restore high voltage channel parameters
- Developing softIOC for Phoebus alarm system
  - ★ Developed a Python program to create the database records for the front and back crystal zone temperatures
  - ★ Developing a Python program to provide random values in conjunction with the softIOC
- Tested alarm support for EPICS base V3.14 array records
- Investigated softIOC implementations that could support alarms on arrays

## **Hall D – JEF**

*Mindy Leffel*

- Populated 20 PMT bases

## **EIC**

*Brian Eng, Pablo Campero, George Jacobs, and Marc McMullen*

- Started reassembly of test station controls system using a National Instruments cRIO 9067, 8-channel, programmable, automation controller
- Started upgrading the test station controls and monitoring software
  - ★ An additional RTD will be located on the heater pipe
- Ordered a 1500-W mineral oil immersion heater, which will be controlled by the software instead of a traditional thermostat
- Set up *Ansys Fluent* to perform thermal simulations of the test stand beampipe
  - ★ Ran simulation with air flow velocity of 1.6 m/s
  - ★ Analyzing results
- Reviewed CAD model provided by LANL with new engineer Chinmay Andhare

## **EIC-DIRC**

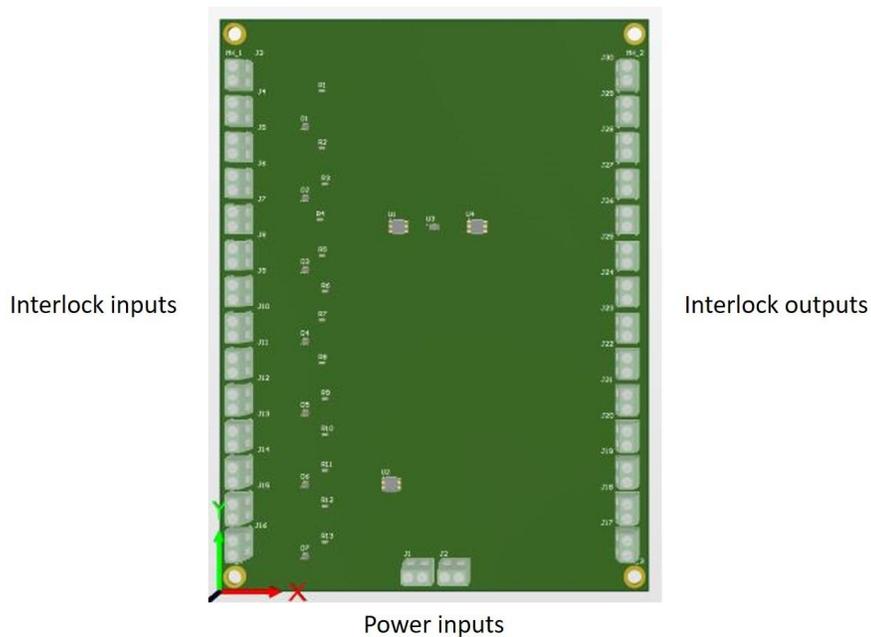
*Tyler Lemon and Marc McMullen*

- Continued PCB layout of the laser interlock board
  - ★ Board dimensions are 8" x 6"
  - ★ Four trace layers and two plane layers
  - ★ Completed placement of all input and output terminal blocks

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- Simulated circuit options for photodiode readout
  - ★ Passive current-to-voltage converter reads voltage drop over a known resistance
  - ★ Active transimpedance amplifier uses an operational amplifier to convert current to voltage
    - Better option, with lower input impedance and isolation for output
  - ★ With either option, to reduce the signal caused by the laser power's noise to below the resolution of the ADC, a passive RC low-pass filter could be used or noise could be eliminated in software by taking and averaging multiple samples

## DSG Website

Peter Bonneau

- Reformatted the [staff](#) and the [publications](#) webpages
- Edited the main [DSG webpage](#), [weekly reports](#), and [monthly memos](#) so links go directly to their lists and preserve the login password requirement